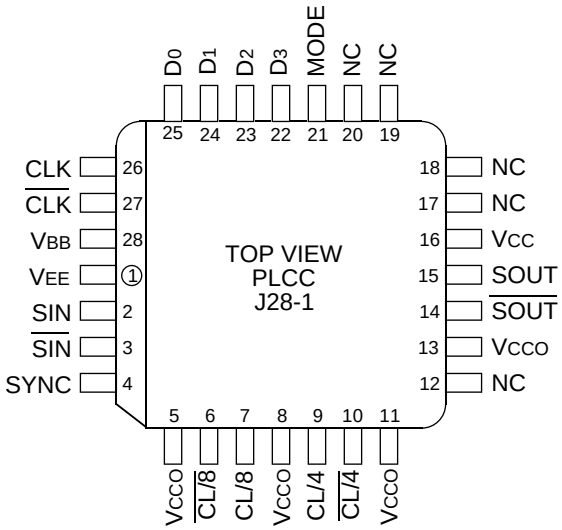
查询SY100E446JC供应商

4-BIT PARALLEL-TO-SERIAL CONVERTER

FEATURES

- On-chip clock ÷4 and ÷8
- Extended 100E V_{EE} range of –4.2V to –5.5V
- 1.6Gb/s typical data rate capability
- Differential clock and serial inputs
- VBB output for single-ended use
- Asynchronous data synchronization
- Mode select to expand to 8 bits
- Internal 75KΩ input pulldown resistors
- Fully compatible with Motorola MC10E/100E446
- Available in 28-pin PLCC package

PIN CONFIGURATION



DESCRIPTION

The SY10/100E446 are integrated 4-bit parallel-to-serial data converters. These devices are designed to operate for NRZ data rates of up to a minimum of 1.3Gb/s. The chips generate a divide-by-4 and a divide-by-8 clock for both 4-bit conversion and a two-chip 8-bit conversion function. The conversion sequence was chosen to convert the parallel data into a serial stream from bit D_0 to D_3. A serial input is provided to cascade two E446 devices for 8-bit conversion applications.

The SYNC input will asynchronously reset the internal clock circuitry. This pin allows the user to reset the internal clock conversion unit and, thus, select the start of the conversion process.

The MODE input is used to select the conversion mode of the device. With the MODE input LOW (or open) the device will function as a 4-bit converter. When the mode input is driven HIGH, the internal load clock will change on every eighth clock cycle, thus allowing for an 8-bit conversion scheme using two E446s. When cascaded in an 8-bit conversion scheme, the devices will not operate at the 1.3Gb/s data rate of a single device. Refer to the applications section of this data sheet for more information on cascading the E446.

For lower data rate applications, a V_{BB} reference voltage is supplied for single-ended inputs. When operating at clock rates above 500MHz, differential input signals are recommended. For single-ended inputs, the V_{BB} pin is tied to the inverting differential input and bypassed via a 0.01µF capacitor. The V_{BB} provides the switching reference for the input differential amplifier. The V_{BB} can also be used to AC couple an input signal.

PIN NAMES

Pin	Function
SIN, $\overline{SIN}$	Differential Serial Data Input
D_0 – D_3	Parallel Data Input
SOUT, $\overline{SOUT}$	Differential Serial Data Output
CLK, $\overline{CLK}$	Differential Clock Input
CL/4, $\overline{CL/4}$	Differential 4 Clock Output
CL/8, $\overline{CL/8}$	Differential 8 Clock Output
MODE	Conversion Mode, 4-bit/8-bit
SYNC	Conversion Synchronizing Input
V_{CCO}	V_{CC} to Output

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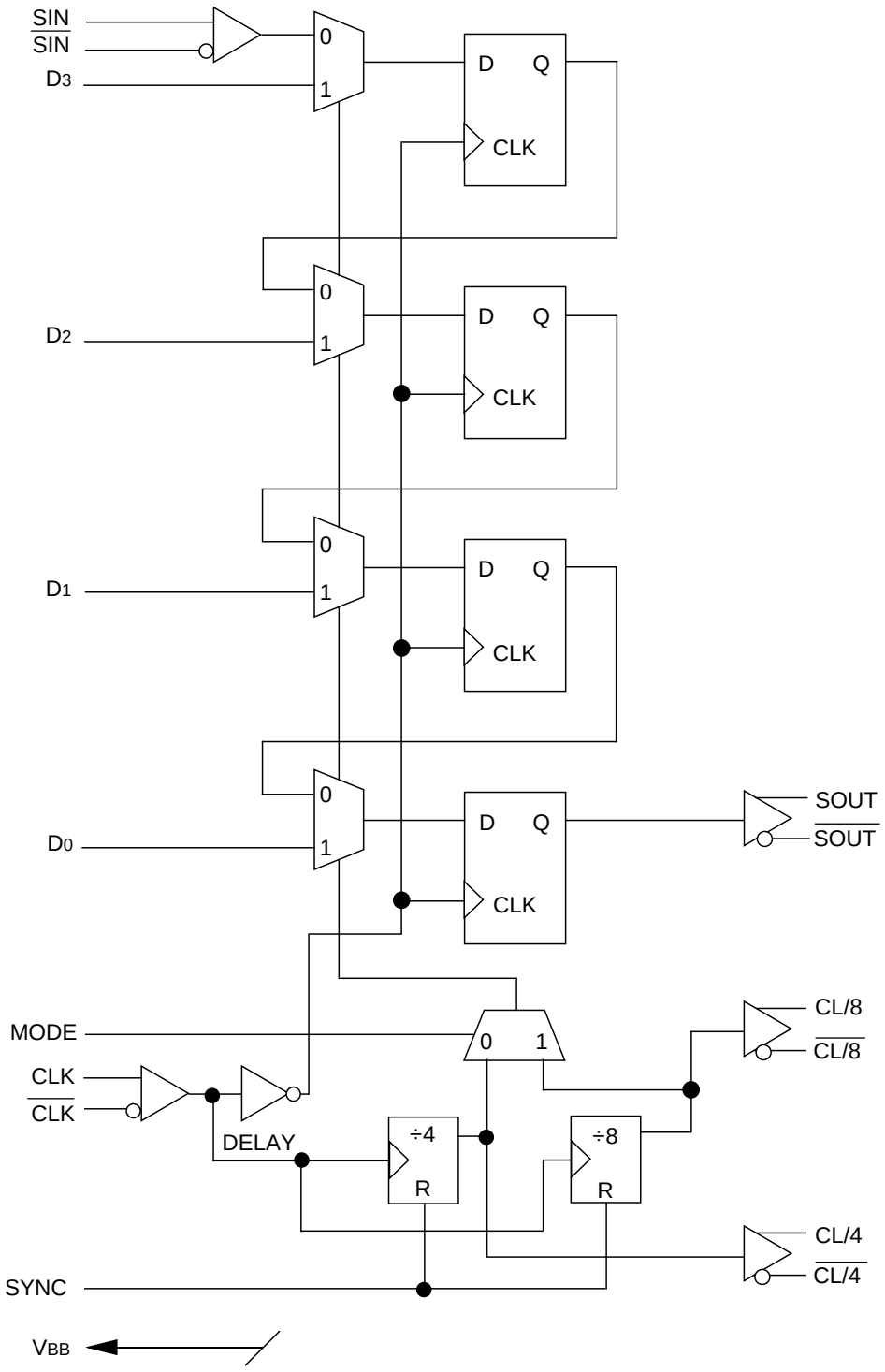
BLOCK DIAGRAM



TRUTH TABLE

Mode	Conversion
L	4-Bit
H	8-Bit

DC ELECTRICAL CHARACTERISTICS

V_{EE} = V_{EE} (Min.) to V_{EE} (Max.); V_{CC} = V_{CCO} = GND

Symbol	Parameter	T_A = 0°C			T_A = +25°C			T_A = +85°C			Unit	Condition
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
I_{IH}	Input HIGH Current	—	—	150	—	—	150	—	—	150	µA	—
V_{OH}	Output HIGH Voltage										V	1
	(SOUT Only) 10E	–1020	—	–790	–980	—	–760	–910	—	–670		
	(SOUT Only) 100E	–1025	—	–830	–1025	—	–830	–1025	—	–830		
V_{BB}	Output Reference Voltage										V	—
	10E	–1.38	—	–1.27	–1.35	—	–1.25	–1.31	—	–1.19		
	100E	–1.38	—	–1.26	–1.38	—	–1.26	–1.38	—	–1.26		
I_{EE}	Power Supply Current										mA	—
	10E	—	110	132	—	110	132	—	110	132		
	100E	—	110	132	—	110	132	—	127	152		

NOTE:

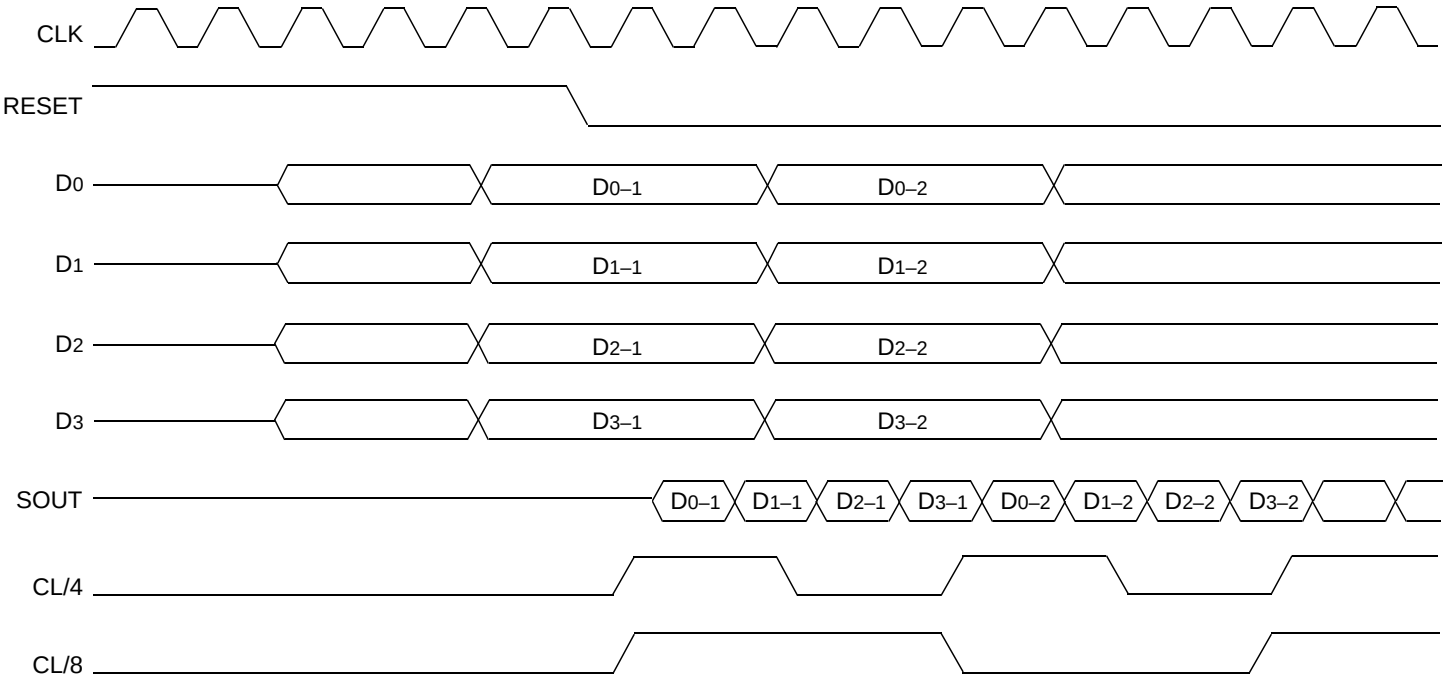
1. The maximum V_{OH} limit was relaxed from standard ECL due to the high frequency output design. All other outputs are specified with the standard 10E and 100E V_{OH} levels.

AC ELECTRICAL CHARACTERISTICS

V_{EE} = V_{EE} (Min.) to V_{EE} (Max.); V_{CC} = V_{CCO} = GND

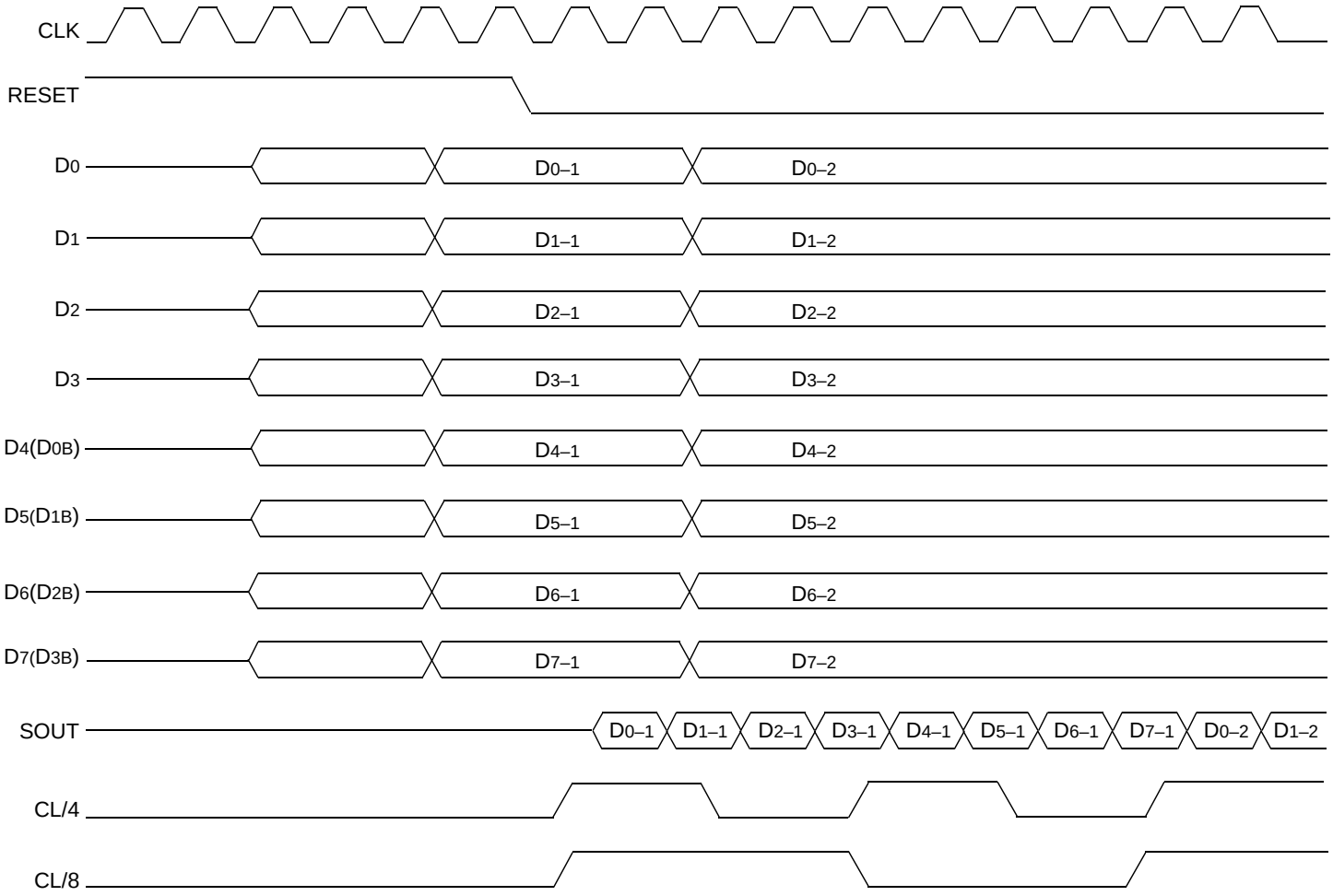
Symbol	Parameter	T_A = 0°C			T_A = +25°C			T_A = +85°C			Unit	Condition
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
f_{MAX}	Max. Conversion Frequency	1.3	1.6	—	1.3	1.6	—	1.3	1.6	—	Gb/s NRZ	—
t_{PLH}	Propagation Delay to Output										ps	—
t_{PHL}	CLK to SOUT	1000	1400	1700	1000	1400	1700	1000	1400	1700		
	CLK to CL/4	500	800	1100	500	800	1100	500	800	1100		
	CLK to CL/8	800	1100	1400	800	1100	1400	800	1100	1400		
	SYNC to CL/4, CL/8	500	800	1100	500	800	1100	500	800	1100		
t_S	Set-up Time										ps	—
	SIN	–200	–400	—	–200	–400	—	–200	–400	—		
	D_n	–200	–400	—	–200	–400	—	–200	–400	—		
	Mode	0	–250	—	0	–250	—	0	–250	—		
t_H	Hold Time										ps	—
	SIN	750	550	—	750	550	—	750	550	—		
	D_n	800	600	—	800	600	—	800	600	—		
	Mode	500	300	—	500	300	—	500	300	—		
t_{RR}	Reset Recovery Time	500	200	—	500	200	—	500	200	—	ps	—
t_{PW}	Minimum Pulse Width CLK, MR	400	—	—	400	—	—	400	—	—	ps	—
t_r	Rise/Fall Time										ps	20–80%
t_f	SOUT	100	225	350	100	225	350	100	225	350		
	Other	200	425	650	200	425	650	200	425	650		

TIMING DIAGRAMS



Timing Diagram A. 4:1 Parallel-to-Serial Conversion

TIMING DIAGRAMS (CONTINUED)



Timing Diagram B. 8:1 Parallel-to-Serial Conversion

APPLICATIONS INFORMATION

The SY10E/100E446 are integrated 4:1 parallel-to-serial converters. The chips are designed to work with the E445 device to provide both transmission and receiving of a high-speed serial data path. The E446 can convert 4 bits of data into a 1.3Gb/s NRZ data stream. The device features a SYNC input which allows the user to reset the internal clock circuitry and restart the conversion sequence (see Timing Diagram A). Note that SOUT is triggered by negative clock edges.

The E446 features a differential serial input and internal divide-by-eight circuitry to facilitate the cascading of two devices to build an 8:1 multiplexer. Figure 1 illustrates the architecture for an 8:1 multiplexer using two E446s (see Timing Diagram B). Notice the serial outputs (SOUT) of the lower order converter feed the serial inputs of the higher order device. This feed through of the serial inputs bounds the upper end of the frequency of operation. The clock-to-serial output propagation delay, plus the set-up time of the serial input pins, must fit into a single clock period for the cascade architecture to function properly. Using the worst case values for these two parameters from the data sheet, t_{PD} CLK to SOUT = 1600ps and t_S for SIN = –200ps, yields a minimum period of 1400ps or a clock frequency of 700MHz.

The clock frequency is somewhat lower than that of a single converter. In order to increase this frequency, it is recommended that the clock edge feeding the E446A be delayed with respect to the E446B, as shown in Figure 2.

Perhaps the easiest way to delay the second clock relative to the first is to take advantage of the differential clock inputs of the E446. By connecting the clock for E446A to the complimentary clock input pin, the device will clock a half a clock period after E446B (Figure 2). Utilizing this simple technique will raise the potential conversion frequency up to the maximum 1.3GHz of a stand-alone E446.

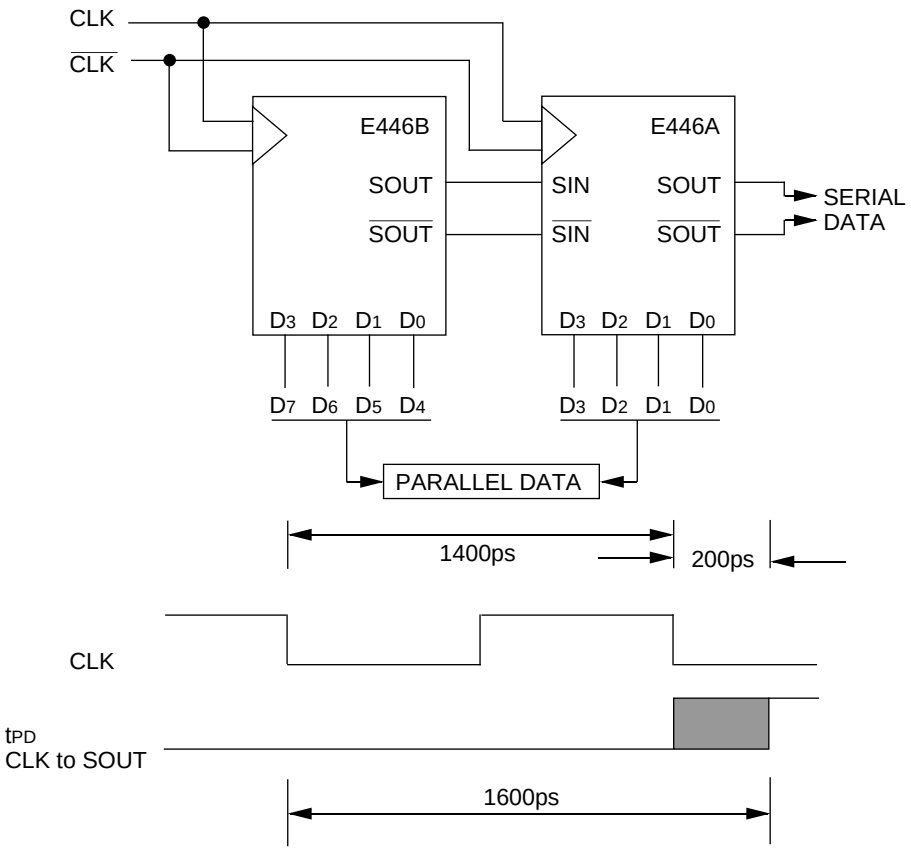


Figure 1. Cascaded 8:1 Converter Architecture

APPLICATIONS INFORMATION

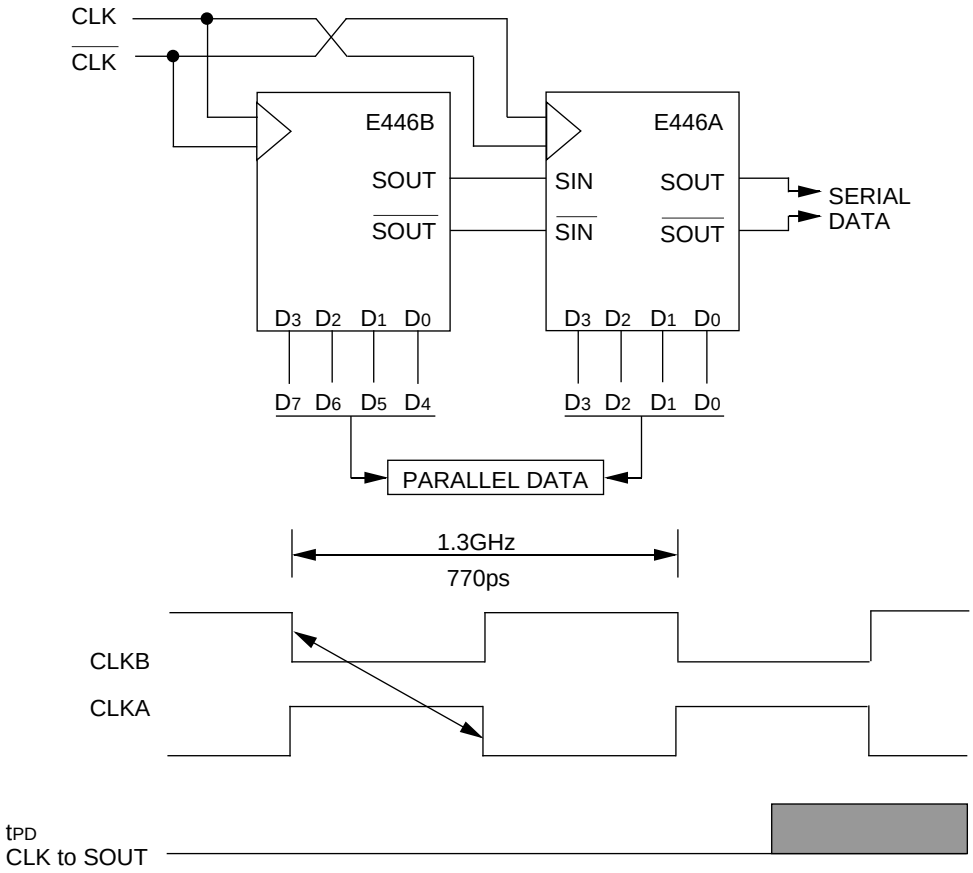
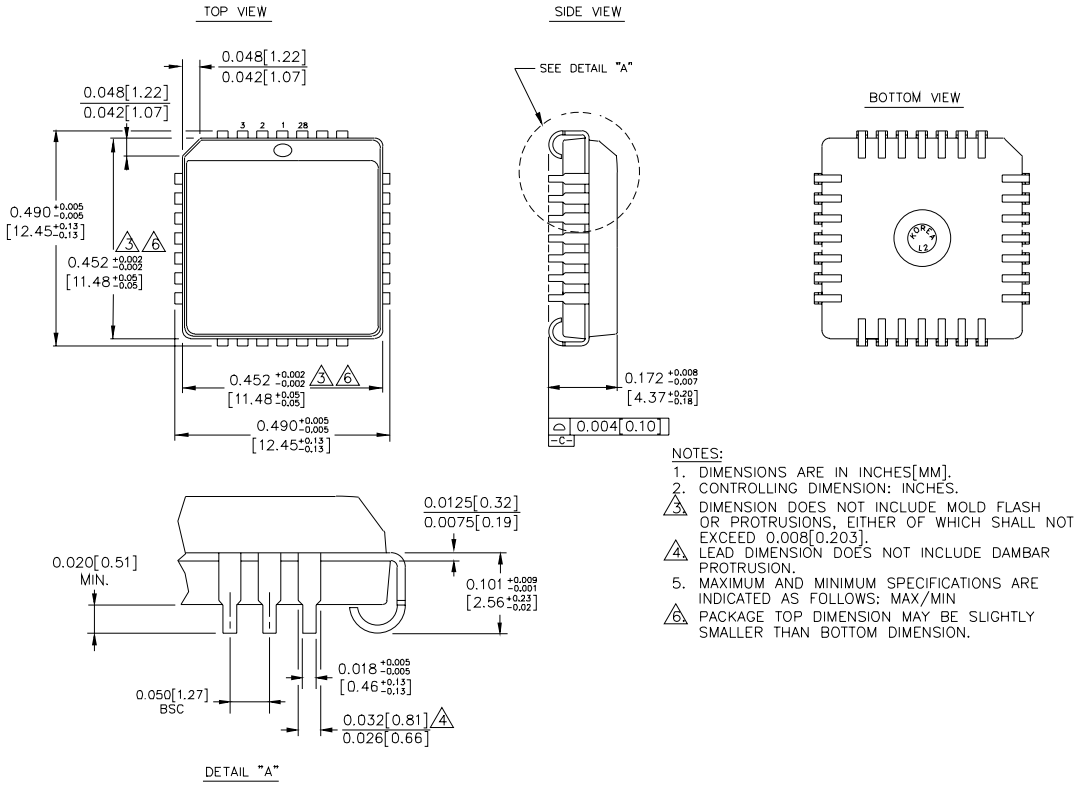


Figure 2. Extended Frequency 8:1 Converter Architecture

PRODUCT ORDERING CODE

Ordering Code	Package Type	Operating Range
SY10E446JC	J28-1	Commercial
SY10E446JCTR	J28-1	Commercial
SY100E446JC	J28-1	Commercial
SY100E446JCTR	J28-1	Commercial

28 LEAD PLCC (J28-1)



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